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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,989	03/01/2002	Cheng Chi Wang	4459-079	1134

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EXAMINER

DUONG, THOI V

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/084,989

Applicant(s)

WANG, CHENG CHI

Examiner

Thoi V Duong

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 ~~is/are~~ pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 ~~is/are~~ rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki et al. (USPN 5,986,204).

As shown in Fig. 4, Iwasaki discloses a sputtering target 407 for forming a metal film from a DC magnetron sputtering apparatus, wherein metal atoms (Ag and Al) of the target 407 are deposited on a substrate 404 (col. 4, lines 35-58) at an atomic percent of Ag equal to or less than 30 at% (col. 4, lines 19-63).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (USPN 6,433,842 B1) in view of Jeong et al. (USPN 6,486,514 B2).

As shown in Fig. 1, Kaneko et al. discloses a thin film transistor (TFT) panel comprising:

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a gate line with a gate electrode 2, 3 on a substrate 1;

a gate insulating layer 4 on the gate line;

a semiconductor layer 5 on the gate insulating layer;

a conductive pattern layer with source and drain electrodes spaced apart on the semiconductor layer, the conductive pattern layer comprising a first molybdenum layer 7, an Al alloy layer 8 on the first molybdenum layer and a second molybdenum layer 9 on the Al alloy layer (col. 7, lines 52-58);

a passivation layer 10 on the semiconductor layer and the conductive pattern layer, the passivation layer having a plurality of contact holes 19; and

a plurality of pixel electrodes 11 on the passivation layer, each of the pixel electrodes extending into one of the contact holes to contact the molybdenum layer 9.

wherein the gate line comprises an Al alloy layer 2 on the substrate and a molybdenum layer 3 on the Al alloy layer (col. 7, lines 17-23).

Kaneko et al. discloses a TFT panel that is basically the same as that recited in claims 1, 2, 17 and 18 except that the alloy layer is not an Ag-Al alloy layer. As shown in Figs. 9 and 10, Jeong et al. discloses that a gate line 22 and a data line 62 with a source electrode 65 and a drain electrode 66 spaced apart on a semiconductor layer 40, are formed of an Ag-Al alloy (col. 8, lines 28-34 and col. 9, lines 1-15). Jeong et al. teaches that the Ag-Al alloy bears low resistance, low melting point and good adhesion characteristics while the Al alloy bears a weak physical or chemical characteristics and erodes easily at the contacting area, when contacting other conducting materials (col. 1, lines 24-40). Thus, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to modify the TFT panel of Kaneko with the teaching of Jeong et al. by employing an Ag-Al alloy for the gate line and the conductive pattern layer so as to provide reliability to the display due to a low resistance and good adhesion characteristics of the alloy.

Claims 3-5, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (USPN 6,433,842 B1) in view of Jeong et al. (USPN 6,486,514 B2) as applied to claims 1, 2, 17 and 18 and further in view of Iwasaki et al. (USPN 5,986,204).

The TFT panel of Kaneko et al. as modified in view of Jeong et al. above includes all that is recited in claims 3-5, 19 and 20 except for the atomic percent of silver in the Ag-Al alloy. As shown in Figs. 1 and 5, Iwasaki et al. discloses an improved back reflecting layer 102 comprising an Ag-Al alloy having a content of silver equal to or less than 30 atomic% (col. 4, lines 19-23 and col. 5, lines 26-37). Iwasaki et al. teaches that a high photoelectric conversion efficiency can be obtained due to a high reflectivity and improved migration resistance of the back reflecting layer (col. 4, lines 24-31). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the TFT panel of Kaneko with the teaching of Iwasaki et al. by forming an Ag-Al alloy containing about equal to or less than 30 at% so as to improve the display brightness.

5. Claims 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (USPN 6,466,280 B1) in view of Iwasaki et al. (USPN 5,986,204).

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As shown in Figs. 5A-5D and 6, Park discloses a liquid crystal display, comprising:

- a top plate comprising a transparent electrode;

- a bottom plate 1 comprising reflective electrodes 68; and

- a liquid crystal layer sandwiched between the top plate and the bottom plate (col. 2, lines 54-57),

wherein an image is generated by the liquid crystal display when ambient light 110 is incident to the surface of the top plate (Fig. 6).

The liquid crystal display further comprises a light source behind the bottom plate (col. 2, lines 54-57) wherein each of the reflective electrodes has at least one aperture 72 defined therein such that an image is generated by the liquid crystal display when light 112 from the light source passes through the apertures of the reflective electrodes.

wherein the bottom plate further comprises (see Fig. 1):

- a plurality of parallel gate lines 6, 8;

- a plurality of parallel data lines 2, 4 formed perpendicular to the gate lines, the gate lines and the data lines being arranged to form a matrix of pixel regions with each of the pixel regions bounded by two adjacent gate lines and two adjacent data lines; and

- a plurality of thin film transistors S formed at intersections between the gate lines and data lines,

wherein each of the reflective electrodes is respectively disposed in one of the pixel regions and functions as a pixel electrode (col. 4, lines 64-67).

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The liquid crystal display of Park et al. includes all that is recited in claims 6-12 except that the reflective electrodes are not formed of an Ag-Al alloy. As shown in Figs. 1 and 5, Iwasaki et al. discloses a reflecting layer 102 comprising an annealed thin film of Ag-Al alloy having a content of silver equal to or less than 30 atomic% (col. 4, lines 19-23 and col. 5, lines 26-67). Also, a reflectivity of greater than 95 % can be obtained for the Ag-Al alloy containing about 90 at% of silver. Iwasaki et al. teaches that a high photoelectric conversion efficiency can be obtained due to a high reflectivity and improved migration resistance of the back reflecting layer (col. 4, lines 24-31). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the TFT panel of Kaneko with the teaching of Iwasaki et al. by forming an Ag-Al alloy containing about 30 at% so as to improve the brightness for the display.

### ***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong  
05/01/2003



TOANTON  
PRIMARY EXAMINER